CLAIMS

What is claimed is:

1. An emulator for emulating a circuit design, the emulator comprising:

a plurality of reconfigurable logic devices each including a plurality of reconfigurable logic elements;

a first reconfigurable logic device of the plurality of reconfigurable logic devices including a first plurality of reconfigurable logic elements clocked by a first clock signal;

a second reconfigurable logic device of the plurality of reconfigurable logic devices including a second plurality of reconfigurable logic elements clocked by a second clock signal; and

wherein an input/output portion of the first reconfigurable logic device and an input/output portion of the second reconfigurable logic device are clocked by one or more signal routing clock signals which are independent of the first and second clock signals.

2. The emulator of claim 1, wherein the first clock signal and the second clock signal are the same clock signal.

3. The emulator of claim 1, further comprising:

at least one interconnect device interconnecting the plurality of reconfigurable logic devices, wherein the input/output portion of the first reconfigurable device is clocked by a

first signal routing clock signal, wherein the input/output portion of the second reconfigurable device is clocked by a second signal routing clock signal, wherein a first portion of the at least one interconnect device is clocked by the first signal routing clock signal, and wherein a second portion of the at least one interconnect device is clocked by the second signal routing clock signal.

4. The emulator of claim 1, wherein the plurality of reconfigurable logic devices comprises a plurality of field programmable gate arrays (FPGAs).

5. The emulator of claim 1, wherein each of the plurality of interconnect devices includes a plurality of multiplexers for time multiplexing data transfers to and from another interconnect device of the plurality of interconnect devices.

6. The emulator of claim 1, wherein a third subset of the plurality of reconfigurable logic devices is clocked at least in part in a third time domain which is different than the first and second time domains.

7. The emulator of claim 1, further comprising a bi-directional data transfer connection, situated between a first reconfigurable logic device of the plurality of reconfigurable logic devices and a first interconnect device of the plurality of interconnect devices, providing simultaneous bi-directional data transfer between the first reconfigurable logic device and the first interconnect device via a single wire or trace.

8. The emulator of claim 7, wherein the first reconfigurable logic device includes a detection logic for determining a signal value asserted by the first interconnect device based at least in part on a voltage level of the bi-directional data transfer connection.

9. The emulator of claim 8, wherein the detection logic is also for determining the signal value asserted by the first interconnect device based at least in part on a signal value asserted by the first reconfigurable logic device.

10. A multi-clocked routing chip for use in an emulation system, the multi-clocked routing chip comprising:

a reconfigurable static routing circuit;

a first set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the first set of input/output circuitry is clocked by a first clock signal; and

a second set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the second set of input/output circuitry is clocked by a second clock signal different than the first clock signal.

11. The multi-routing chip of claim 10, wherein the first and second sets of input/output circuitry each includes a plurality of one-to-n demultiplexers and a plurality of n-to-one multiplexers, where n is an integer greater than 1.

12. The multi-routing chip of claim 10, further comprising a third set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the third set of input/output circuitry is clocked by a third clock signal different than the first and second clock signals.

13. An emulation system comprising:

a first plurality of reconfigurable logic devices;

a second plurality of reconfigurable logic devices;

a third plurality of reconfigurable logic devices;

a first time multiplexed interconnection coupled to and situated between the first plurality of reconfigurable logic devices and the second plurality of reconfigurable logic devices; and

a second time multiplexed interconnection coupled to and situated between the second plurality of reconfigurable logic devices and the third plurality of reconfigurable logic devices, wherein clocking of the second time multiplexed interconnection is independent of clocking of the first time multiplexed interconnection.

14. The emulation system of claim 13, wherein each of the first plurality of reconfigurable logic devices, each of the second plurality of reconfigurable logic devices, and each of the third plurality of reconfigurable logic devices is a field programmable gate array (FPGA).

15. The emulation system of claim 13, wherein the first time multiplexed interconnection includes a first set of input/output circuitry of a multi-clocked routing chip and the second time multiplexed interconnection includes a second set of input/output circuitry of the multi-clocked routing chip.

16. The emulation system of claim 13, wherein the first time multiplexed interconnection includes a first plurality of multiplexers and demultiplexers, and the second time multiplexed interconnection includes a second plurality of multiplexers and demultiplexers.

17. A system comprising:

a first chip;

a second chip; and

a bi-directional data transfer connection, situated between the first chip and the second chip, providing simultaneous bi-directional data transfer between the first and second chips via a single wire or trace.

18. The system of claim 17, wherein the first chip includes a detection logic for determining a signal value asserted by the second chip based at least in part on a voltage level of the bi-directional data transfer connection.

19. The system of claim 18, wherein the detection logic is also for determining the signal value asserted by the second chip based at least in part on a signal value asserted by the first chip.

20. The system of claim 17, wherein the system comprises an emulator and the first chip comprises a first reconfigurable logic device of a plurality of reconfigurable logic devices.

21. The system of claim 20, wherein the second chip comprises a first interconnect device of a plurality of interconnect devices interconnecting the plurality of reconfigurable logic devices.

22. The system of claim 20, wherein the second chip comprises a second reconfigurable logic device of the plurality of reconfigurable logic devices.